Packaging and characterization of orthogonal transfer array CCDs for the WIYN One Degree Imager

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ABSTRACT

The WIYN One Degree Imager (ODI) will provide a one degree field of view for the WIYN 3.5 m telescope located on Kitt Peak near Tucson, Arizona. Its focal plane will consist of an 8x8 grid of Orthogonal Transfer Array (OTA) CCD detectors with nearly one billion pixels. The implementation of these detectors into the focal plane has required the development of several novel packaging and characterization techniques, which are the subject of this paper. We describe a new packaging/hybridization method in which the CCD die are directly bonded to aluminum nitride ceramic substrates which have indium bump on one side and brazed pins on the other. These custom packages allow good thermal conductivity, a flat imaging surface, four side buttability, and *in situ* testing of the devices during backside processing. We describe these carriers and the backside processing techniques used with them. We have also modified our cold probing system to screen these OTA die at wafer level to select the best candidates for backside processing. We describe these modifications and characterization results from several wafer lots.

Keywords: detectors, CCDs, telescopes, imaging

1. INTRODUCTION

The WIYN Observatory (Wisconsin, Indiana, Yale, NOAO) is developing a very large imaging instrument called the One Degree Imager (ODI) for its 3.5 m telescope on Kitt Peak in Arizona[1]. A top priority of this instrument is to obtain the highest possible image quality. For this reason the CCD detectors were chosen to be Orthogonal Transfer Arrays (OTA) which are capable of compensating for image movement caused mainly by the Earth's atmosphere[2,3]. The University of Arizona's Imaging Technology Laboratory (ITL) has developed a process to create a backside illuminated version of the STA2200 OTA CCD designed and developed by Semiconductor Technology Associates, Inc. (www.sta-inc.net). The various aspects of the detector development program for ODI are discussed in this paper.

The overall process for producing the focal plane mosaic is described next. The CCD devices are designed by and fabricated through STA. They test the devices on a wafer prober for DC shorts and perform room temperature imaging. Wafers are shipped to ITL and tested at -60 C on a wafer prober. Gold stud bumps are applied to all detector bond pads. Wafers are next backside lapped by an external vendor and diced in-house. Good die are then hybridized to the substrate. *In situ* testing is possible at this point by installing the hybrids into the test dewar and imaging the thick detectors (typically by only analyzing dark current images). Hybrids are backside etched and oxidized. They are next packaged by attaching the mounting/cooling frame and then backside coated using the ITL Chemisorption Coating process. The devices are characterized in a dewar at -100 C and stored until all devices are ready for assembly onto the focal plane baseplate. Assembly will take place in late 2009 at ITL and then the full mosaic will be tested by WIYN before installation at the telescope in early 2010.

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2. PACKAGE DESIGN

A focal plane mosaic in an instrument requires a close butting of the individual detectors, each mounted flat (< 20 µm peak-valley) and coplanar with each other. Good thermal conductivity from the cooling mechanism to the silicon detector is also required. Because OTA devices consume a relatively large amount of power due to their internal logic, this latter requirement is more critical than for some other astronomical mosaics. We have based our design of the ODI package on our previous work using what we call Fully Buttable Imagers (FBI) technology.[4,5]

Our package design consists of the silicon detector die hybridized to a ceramic substrate. The standard process we have used for many years makes use of a silicon substrate rather than ceramic. We use aluminum nitride (AlN) as the ceramic of choice since it has good thermal conductivity, can be readily fabricated with multilayers and input/output (IO) pins, and can be well polished for flatness and surface quality control. For this particular design we have chosen to use brazed pins on the underside of the ceramic for signal IO. Previous versions have utilized metal pads which require later attachment of a connector with solder or conductive epoxy. The pins represented a major backside processing challenge since all subsequent tooling had to be modified to accommodate the pinned hybrids rather than flat hybrids. The advantage is that in-house connector attachment is not required and the devices may be tested immediately after hybridization if desired.

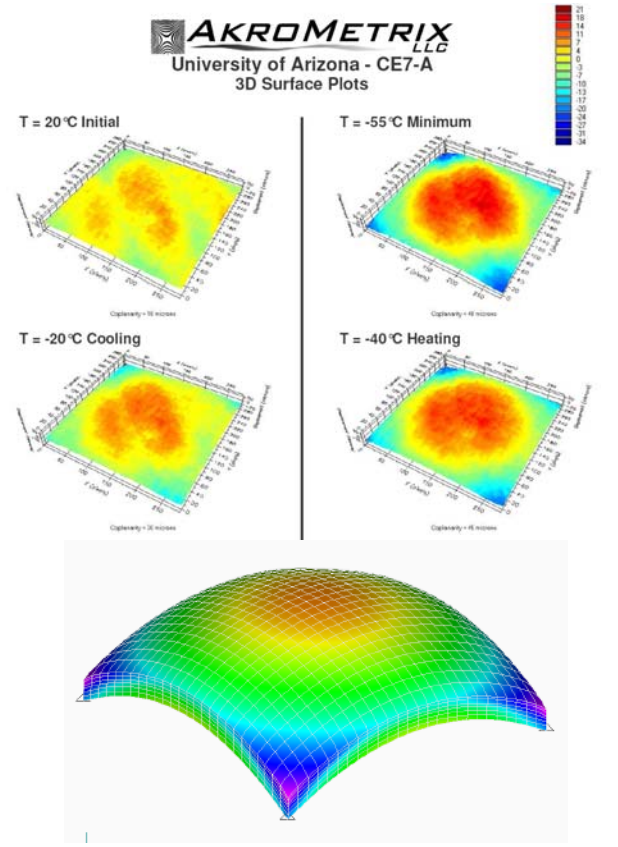

Figure 1. (top) Measured profile change of a mock-up package cooling from room temperature to -55 C (30 µm amplitude). (bottom) FEA model profile of a CE6 package cooled to -100 C (20 µm amplitude).

The indium bumps are deposited on the ceramic topside bond pads by a different vendor than the ceramic manufacturer. Careful consideration had to be given to utilize compatible metallization for the different vendors. The indium deposition proved to be a difficult problem, especially considering we require relative tall bumps (20 µm). Initial contracts were made with two vendors for development, and one was finally selected which was able to provide excellent results.

A frame is attached to the underside of the substrate to provide mechanical mounting and a thermal path from the bottom (mounting) side of the frame to the ceramic substrate. We have previously used Invar-36 for these frames but chose a silicon-aluminum alloy called Osprey CE5 for this project. This decision was made in consultation with the ceramic vendor as well as based on finite element analysis models performed at WIYN. The CE5 material has good thermal conductivity (110 W m^{-1} K^{-1}), low density (2.35 g cm^{-3}), and a relatively good match of thermal expansion to silicon and AlN (5 x 10^{-6} C^{-1}). We show in Figure 1 finite element analysis results of the expected shape of the imaging surface when cooled to -100 C. As a verification that the models were at least close to reality, we built a mock up device before the ceramics were ordered and contracted a vendor to make some surface profile measurements while cooling to -55 C, also shown in Figure 1. The model and experimental results matched reasonably well. We note the models and mock up tests did not use exactly the same materials as our final material choices since at the time of modeling it was not clear which Osprey alloys would be available. The CE5 material chosen for the final design will perform better than the mockup and FEA models since it has a closer expansion coefficient to silicon than the earlier material. The CE5 is gold plated by the vendor in order to reduce emissivity and provide a more uniform bonding surface. We also note that the CE5 material is machined by the vendor rather than in-house in our machine shop. There is some expertise required to properly fabricate the parts without inducing stress or micro fractures, which we felt was best maintained by the vendor. The final package is shown in Figure 2.

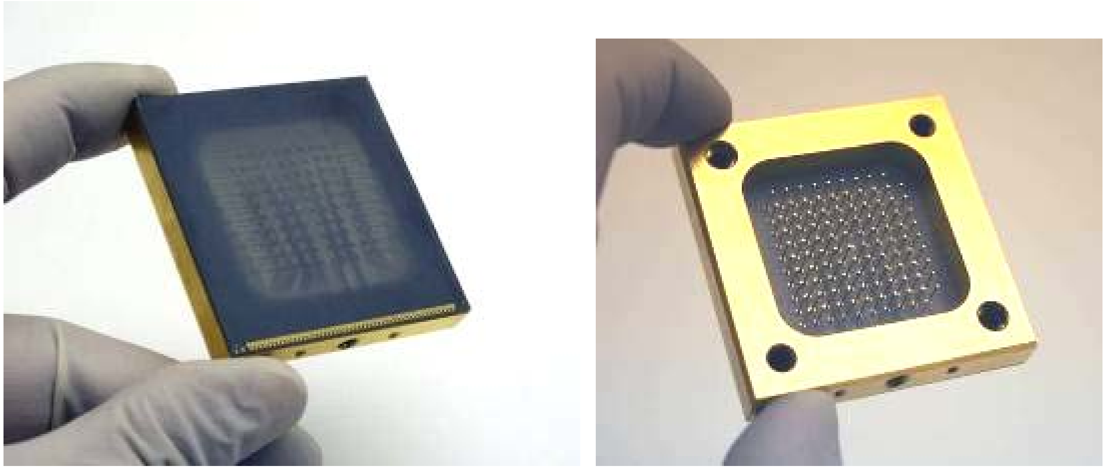

Figure 2. The final ODI package, shown topside at left and bottom side with the CE5 frame attached at right. The AlN is seen to be translucent, showing internal traces and vias. The indium bumps are on the lower side on the top. The bottom pin grid has one missing pin as an orientation key.

3. BACKSIDE PROCESSING

After cold wafer probing, which is discussed in the next section, gold bumps are placed on each CCD bond pad. This bumping process is performed with a high speed Kulicke and Soffa ATPremier stud bumping machine. After bumping the wafers are sent to a vendor for mechanical backside grinding to 250 µm thickness. They are next diced in house, cleaned, and the known good die are ready for hybridization.

The hybridization of the silicon detectors onto the substrate is performed with a new bonder developed in-house which is shown in Figure 3. The bonder was developed to experiment with new hybridization technologies such as used here for ODI. The bonding to pinned packages is a novel technique and allows the flexibility to test devices immediately after or even during hybridization. This is useful for optimizing the bonding process as well as eliminating subsequent lost time when processing a device which has failed during bumping, lapping, dicing, or hybridization. The bonding process itself is very similar to other devices we process. Typical bonding consists of mounting the detector on the upper chuck and the substrate with pins on the lower chuck, optical alignment, bonding for 20 minutes, and release. Epoxy underfill is then performed to provide mechanical support. The underfill movement between the die and substrate is slower with ceramic than silicon. The cure time is over night, so the devices are then ready for etching the next day.

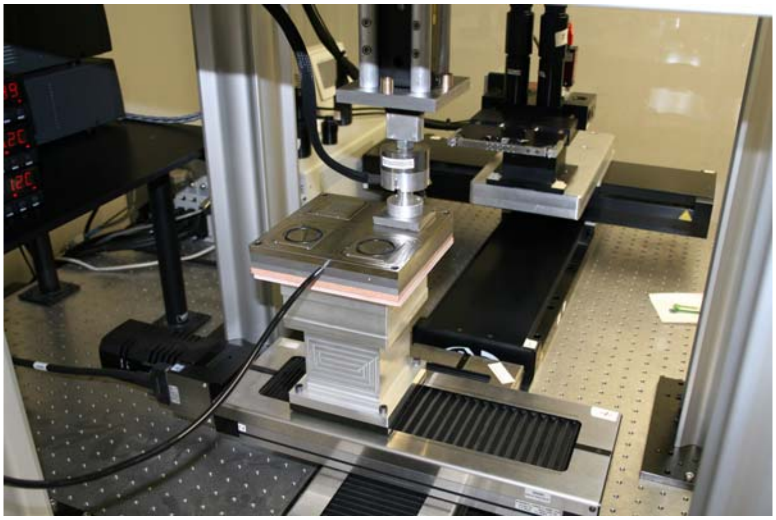

Figure 3. The custom bonder used for ODI hybridization. The lower chuck can hold either one or two OTA CCDs. The detectors rest on the black o-rings (bumps down) while the pinned substrates sit next to them where the upper chuck can be seen bonding one device.

After hybridization (and optional testing), the devices are backside etched. All ODI silicon is epitaxial material although the resistivity and epitaxial thickness has varied over the different lot runs for evaluation purposes. The etching technology used is the same as previous backside work at ITL, but the tooling is highly specialized for the pinned package. We show in Figure 4 a device being etched in acid. The CCD is installed in a thick ceramic supporting block which rests on a Teflon holder. The pins are embedded in the block and sealed by wax to avoid exposure to the acid. This waxing process has proved more difficult than standard substrate waxing, but can still be performed efficiently in a production process.

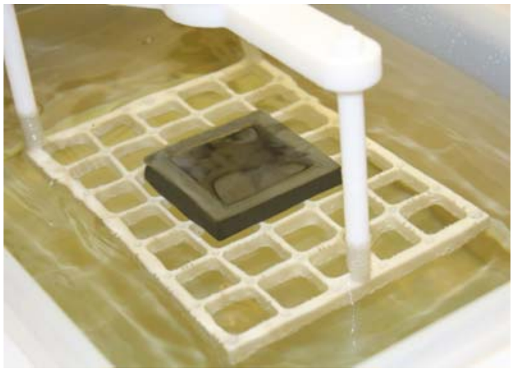

Figure 4. An ODI CCD as it is etching in acid.

After etching, the device is oxidized and then Chemisorption coated for enhanced quantum efficiency. The coating process is similar to previous work, although again new tooling has been made to support the pinned hybrid in the vacuum chamber. The antireflection (AR) coating is tailored to the scientific requirements of the ODI project. The final QE of the devices is the same as that achieved by any other CCD with the same silicon type and AR coating.

After coating, the device is packaged, which in this case is the attachment of the CE5 frame to the underside of the ceramic substrate. This must be done in a precision jig to ensure that the imaging surface of each detector is flat and at the same height relative to the bottom of the CE5 mounting surface. The jig used is shown in Figure 5. The top (backside) surface of the CCD is held against a perforated, static-dissipating ceramic plate (Cerastat-Z) and the frame is placed on the base of the jig. Bearings guide the top chuck downward such that the bottom of the ceramic bonds to the top of the frame, to which epoxy has been applied. The final imaging surface height is set by precision gauge pins to a tolerance of about 1 μm relative to the bottom of the frame. After a room temperature cure in the jig the packaged device is placed in an oven for final curing. After this the device is ready for final characterization.

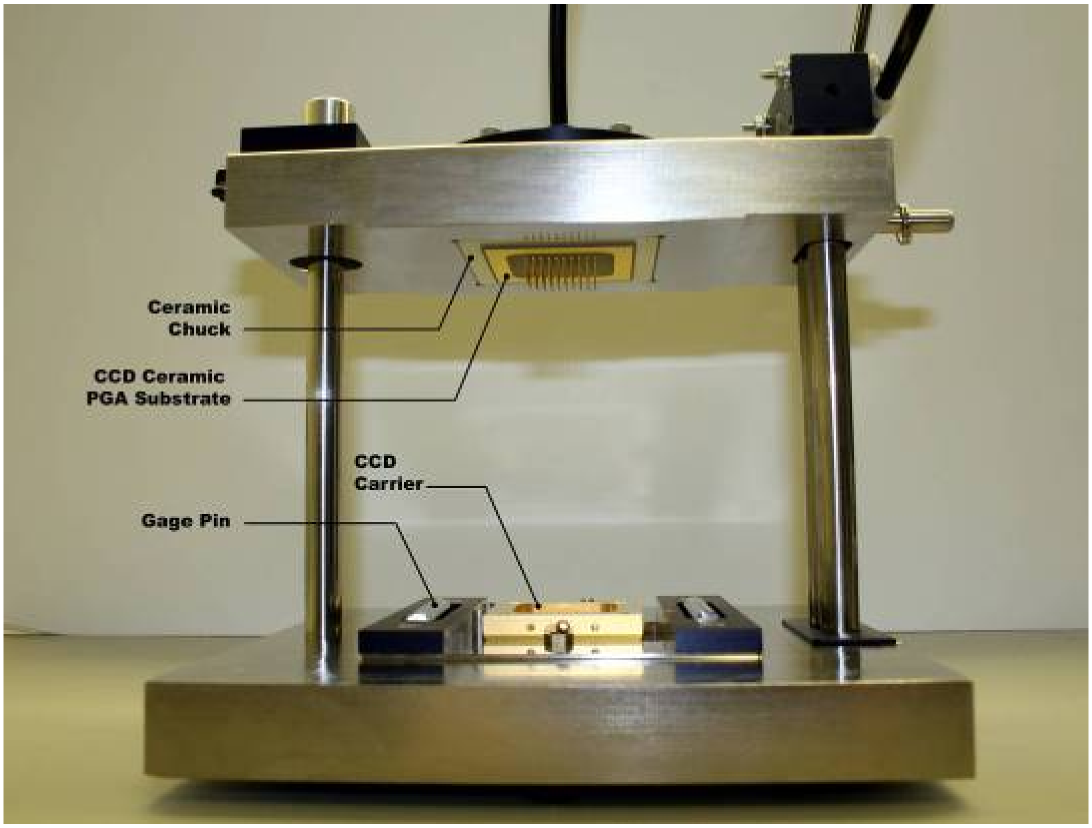

Figure 5. The packaging jig for the ODI CCDs. The hybridized detector can be seen held by vacuum on the upper porous ceramic chuck. The CE5 frame is on the lower base.

4. DETECTOR CHARACTERIZATION

Detector characterization is critical to the ODI project success. The individual devices must be characterized as they are produced before assembly into the final focal plane mosaic. Good devices are stored waiting for insertion in the focal plane base plate and poor devices must be replaced. Testing is required both at the wafer level (screening) and after backside processing. The equipment developed for automated testing includes a cold wafer probe system, a large test dewar, two 8-channel controllers, and an optical testing bench[6,7]. We describe these in this section.

4.1 Camera controllers

At ITL we use Astronomical Research Corporation, Inc. (ARC) CCD controllers for all detector characterization (http://www.astro-cam.com). For the ODI devices we have replaced the two dual-channel ARC-45 video boards with one of the newer ARC-48 eight channel video boards. We use the ARC-22 “Gen3” timing board and two ARC-32 clock boards per system. One clock board drives the CCD clocks (serials and parallels) and one clock board drives the on-chip OTA logic.

Significant effort was spent developing DSP assembly code to operate the OTA devices using the ARC controllers. This was aimed at operating the devices with the same higher level testing software we use for all astronomical devices rather than requiring special modifications for OTAs. This was successful and we operate the OTA devices in exactly the same manner as we do multi-amplifier non-orthogonal transfer devices. Data from each of the eight video outputs is written to a FITS image extension and can be displayed directly with a standard astronomical image viewer such as SAO’s ds9.

We note that initial testing at STA used both the NOAO Monsoon controller[8] as well as proprietary STA controllers. The final ODI instrument will use the STARGRASP controller[9] developed at the University of Hawaii (http://www.stargrasp.org).

4.2 Cold wafer probing for prescreening

Initial room temperature wafer probing was performed at Semiconductor Technology Associates, Inc. Cold wafer probing was subsequently performed at ITL. The ITL Cold Wafer Probing System consists of an Electroglas 2001x automated wafer prober equipped with a Temptronic 6" cold chuck, a controlled environmental enclosure, a Keithley switching system, and the ARC controller. The wafer prober has an automated material handling unit capable of testing 25 wafers per cycle. Testing was performed at -60 C using the closed cycle refrigeration unit. The Controlled Environment Enclosure (CEE) is used to maintain light tight and low humidity conditions near the wafers and other cold components in the system.

The DC test system consists of a 400 channel Keithley 7002 matrix switching system and Keithley test meters capable of measuring resistance, voltage, and current between all probe contacts. The DC test system is under the control of a National Instruments LabVIEW program written in-house. This allows downloading of any number of test files for specific characterization requirements. All data are written to an Excel spreadsheet for analysis and archiving.

Figure 6 shows an image from an ODI CCD taken on the probe station. The projected grid pattern was

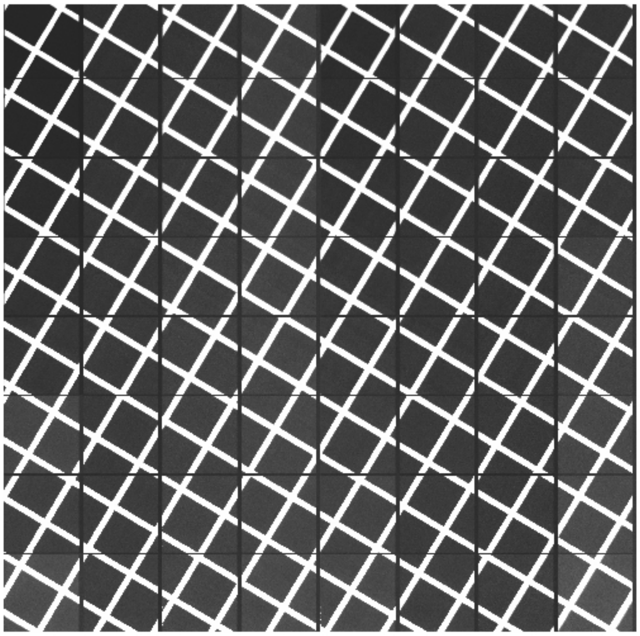

Figure 6. An image from an ODI OTA CCD taken at -60 C. The projected grid pattern is useful to ensure the address logic is correctly operating and that also cells function properly.

found to be useful when developing the cell addressing code for the OTA devices. An LED driven woven fiber optic uniform illumination panel and an Fe55 X-ray source are also available for image testing on the probe station.

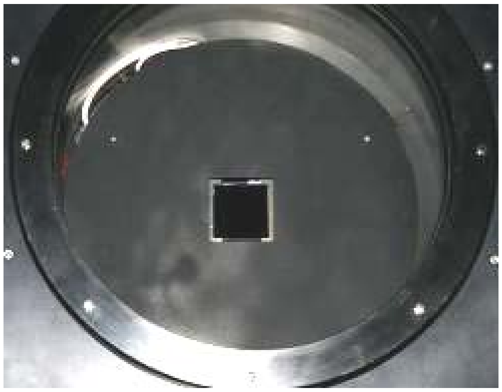

Figure 7. A backside illuminated STA2200 OTA CCD installed in the test dewar, looking in through the window. The dewar is designed to test up to four OTA devices during one cold cycle.

4.3 Final detector characterization

A second optical bench has been installed in our detector characterization lab to support testing with a new large dewar capable of testing multiple CCDs per cold cycle. An ODI CCD in the dewar is shown in Figure 7 and the optical bench can be seen in Figure 8. All optical components are mounted on a 4'x6' optical table. The Big Universal Dewar (BUD) handling cart attaches to the table which has an ESD-safe, opaque enclosure over the tabletop which was custom-built by Newport Optics to our requirements. A 150 mm diameter flat steering mirror is mounted on a rotary stage. This mirror may be used to direct to the detector light from either the integrating sphere or a lens arrangement projecting the screen of a 17" diagonal LCD monitor. Test patterns are generated using the LCD monitor, which is connected to a PC. The flexibility of this system has proven to be very useful for a wide variety of testing situations. These test patterns are very useful for ensuring the proper mapping of multi-channel data when developing code, for estimating cross talk, and measuring relative performance of the different video channels. The optical system focuses an image of the monitor onto the CCD using a lens mounted on a linear stage. The characteristics of the current optical system image a monitor pixel to about 80 microns in size at the dewar focal plane. We note the prober illumination system currently uses a glass mask rather than an LCD monitor for its projected images. Uniform illumination is provided by a small UV coated integrating sphere with a one-inch aperture. The illumination is uniform to 1% over the 300 mm focal plane diameter. Quasi-monochromatic light suitable for QE measurement is provided by a quartz-halogen incandescent lamp operated with a photo-feedback controller for regulated light output and a series of three 6-position filter wheels equipped with narrow band pass filters from 350 to 1050 nm. An image taken with this system from the first backside thinned ODI device in the final package is shown in Figure 9. This device has a serial

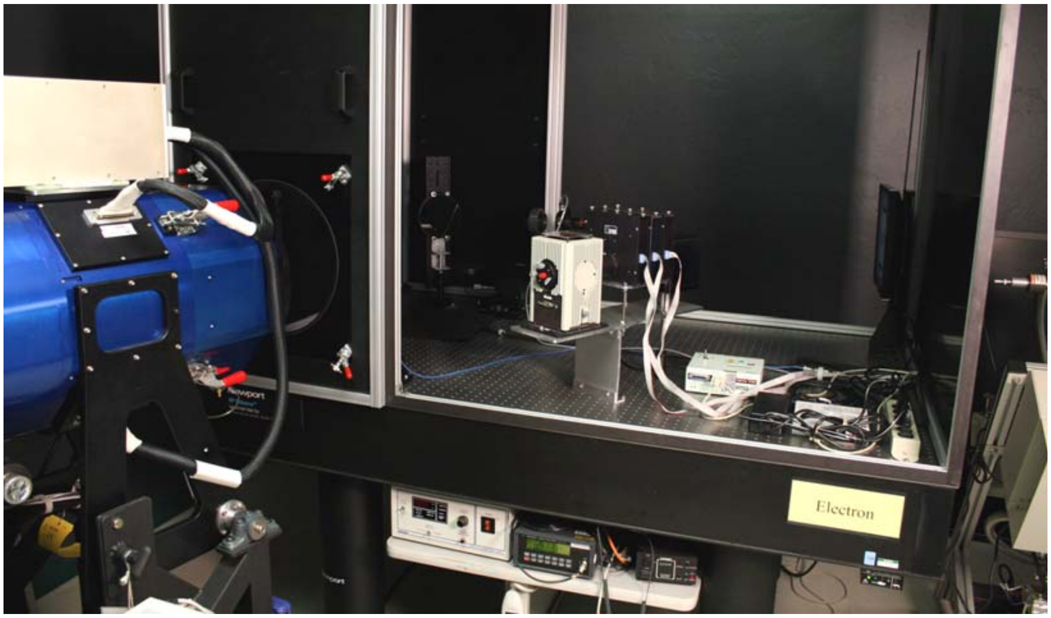

Figure 8. The detector characterization bench used for ODI device testing. The dewar is at left looking into the optical enclosure which has a front cover and internal baffles removed. The LCD monitor is at the back right and the quartz lamp and filters wheels can be seen in the front center. The mirror and lenses are in the back left.

short which causes some cells to be smeared. It can be seen that testing with a grid pattern is an excellent way of determining such defects.

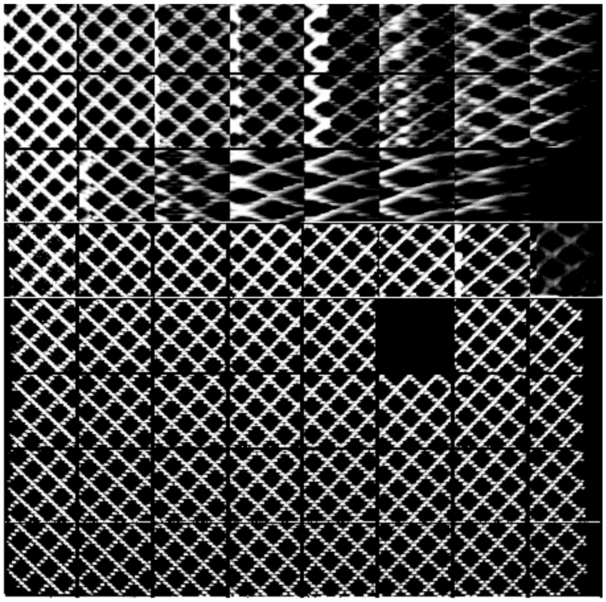

Figure 9. An image of a grid from the first backside ODI device in the final ODI package, taken in the test dewar at -100 C. The serial CTE is due to an inter-serial short in this device.

Python and LabVIEW are used to control all instrumentation and the controller functions. The main use of the scripts is to provide unattended operation so that data acquisition may occur in the night with no lab staff present. Current scripts include the following functions: quantum efficiency, standard photon transfer curve sequence, photo transfer curve via ramp images, Fe-55 x-ray image acquisition, pocket pumping, transfer curves (optimization of bias voltages for gain and noise), linearity, and acquisition of complete image sets (zeros, flats, darks, Fe-55). All image data is stored in Multi-Extension FITS (MEF) files.

In addition to electro-optical characterization, the project requires several mechanical measurements to be made. The critical issues are individual device flatness and overall mosaic focal pane flatness. We use two different measurement systems for these tests. A MicroMeasure 3D non-contact profilometer is used to measure the individual device surfaces. It uses interchangeable optical pens to achieve a wide variety of resolutions. We show one measure of the first backside device in the final package in Figure 10. The overall surface flatness is about 10 μm peak-valley. The specification is better than 20 μm at operating temperature. The assembly of the 64 devices on to the focal plane base plate will take place at ITL and the final surface profile will be measured with a Summit VIEW 600 non-contact coordinate measuring machine. We show in Figure 11 the ODI SiC focal plane base plate as received from the manufacturer on the VIEW during an initial test of its profile.

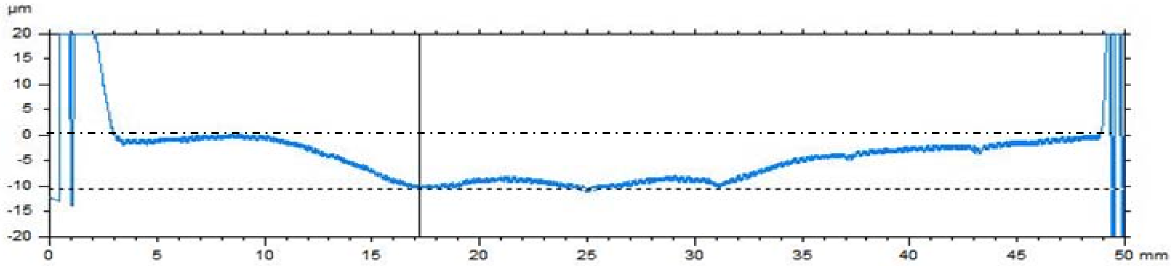

Figure 10. A surface profile measured from the first backside ODI CCD in the final package. The total flatness is about 10 μm peak to valley at room temperature. This data was taken with a MicroMeasure 3D non-contact profilometer.

Figure 11. The VIEW Summit 600 coordinate measuring machine with the ODI SiC base plate under initial test. The flatness was measured to be about 10 µm peak-valley, as received.

5. SUMMARY

We have developed a new buttable detector package and corresponding back illuminated device processing flow for the STA2200 Orthogonal Transfer Array CCD. The first backside devices have been processed and are working successfully. During 2009 we will complete the 64 detectors needed to assemble the final focal plane. First light of the complete One Degree Imager will be in 2010. Methods of operating the devices with the ARC controllers, cold wafer probing, hybridization directly to ceramic with brazed pins, etching, backside coating, and final packaging have all been developed and tested. Fully automated detector characterization equipment and software has been installed and is ready for production testing of the devices as they are fabricated. We expect the testing rate to be 2-3 devices per week. Up to four devices may be cooled at once if required. The SiC focal plane base plate for ODI has been measured for initial flatness and found to meet specifications.

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