

The Orthogonal-Transfer Array: A New CCD Architecture for Astronomy*

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ABSTRACT

The orthogonal-transfer array (OTA) is a new CCD architecture designed to provide wide-field tip-tilt correction of astronomical images. The device consists of an 8×8 array of small (~500×500 pixels) orthogonal-transfer CCDs (OTCCD) with independent addressing and readout of each OTCCD. This approach enables an optimum tip-tilt correction to be applied independently to each OTCCD across the focal plane. The first design of this device has been carried out at MIT Lincoln Laboratory in support of the Pan-STARRS program with a collaborative parallel effort at Semiconductor Technology Associates (STA) for the WIYN Observatory. The two versions of this device are functionally compatible and share a common pinout and package. The first wafer lots are complete at Lincoln and at Dalsa and are undergoing wafer probing.

Keywords: CCD, OTCCD, orthogonal-transfer CCD, Pan-STARRS, WIYN, tip tilt

1. INTRODUCTION

The orthogonal-transfer CCD (OTCCD) is a device capable of shifting charge in all directions and was developed for compensating the image motion across a sensor in situations where motion of the scene or the sensor platform during image integration would otherwise lead to blur.¹ The principal application of this device to date has been in ground-based astronomy, where the device has been shown to be effective in removing random image motion due to atmospheric-induced phase distortion as well as telescope shake.² In effect, the OTCCD can perform the so-called “tip-tilt” correction electronically, resulting in improved image resolution and S/N.

A tip-tilt correction can only be usefully applied over a patch of sky characterized by the isokinetic angle, which depends on the altitude of the disturbed air above the telescope but is typically of the order of a few arc minutes. To use the OTCCD for wide-field imaging requires arrays of independently controlled devices, in effect, a “rubber focal plane” in which an optimum shift pattern can be applied independently to each OTCCD subarray. A first demonstration of this concept was the so-called OPTIC camera consisting of two abutted 2K×4K OTCCDs.³ Each of these CCDs comprised two 1536×2048 sections for science image acquisition in the chip center and 512×2048 sections at the top and bottom for guide-star tracking. Serial registers along the top and bottom provided readout for both the star-trackers and science images. Thus the chip pair consisted of four independent imaging sections and four star-tracker sections.

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An extension of this approach was described a few years ago where the imagers consisted of an integrated 2D array of small OTCCDs, each independently controllable via on-chip addressing logic.⁴ This sensor has been named the OTA (Orthogonal Transfer Array), and the U. of Hawaii Institute for Astronomy has elected to pursue the development of this sensor in collaboration with MIT Lincoln Laboratory for use in Pan-STARRS (Panoramic Survey Telescope and Rapid Response System).⁵ Pan-STARRS will comprise four 1.8-m telescopes, each equipped with a 1-Gpixel focal plane consisting of 64 OTAs.

The WIYN (Wisconsin, Indiana, Yale, NOAO) observatory has joined UH-IFA as a collaborator in the OTA development to support its goal of a similar focal plane called the ODI, or one-degree imager, for the WIYN telescope on Kitt Peak.⁶ WIYN is contributing to this device development by funding the design of a second source of OTAs at Semiconductor Technology Associates (STA) in San Juan Capistrano, CA and fabrication at Dalsa Semiconductor. The Lincoln and STA designs were jointly carried out to share common design features, be functionally compatible, and use a common package and pinouts. This strategy of a parallel development effort ensures a backup source for a chip that is novel in its architecture and more complex than traditional scientific CCD imagers.

This paper describes the key features of the first prototype OTAs, as well as the four-side-abutable package and focal plane layout for Pan-STARRS and the WIYN ODI.

2. DEVICE ARCHITECTURE AND OPERATION

Figure 1 illustrates the basic building blocks of the device. The detector consists of an 8×8 array of OTCCD subarrays or cells (left), each cell in turn comprising an array of about 500×500 pixels (center) and a serial readout register. The pixels are four-phase OTCCD structures with one of the two designs shown in the right side of Figure 1. Associated with each OTA cell is a control-logic block which is used to control the four parallel phases, P1–P4, and the video output signal of each cell. Each logic block can be addressed and loaded with data bits that a) determine whether the parallel clocks are stationary (during integration) or shifting charge, and b) enable/disable the output-amplifier connection to the video output bus. These features are described in more detail later. To maximize fill factor, the cells are abutted as closely as permitted by the process technology, and all I/O leads are confined to one edge of the device. The die size is 49.5×49.5 mm, a size that was chosen on the basis that a 150-mm wafer (the size used in both the Lincoln and Dalsa facilities) can just accommodate four such devices.

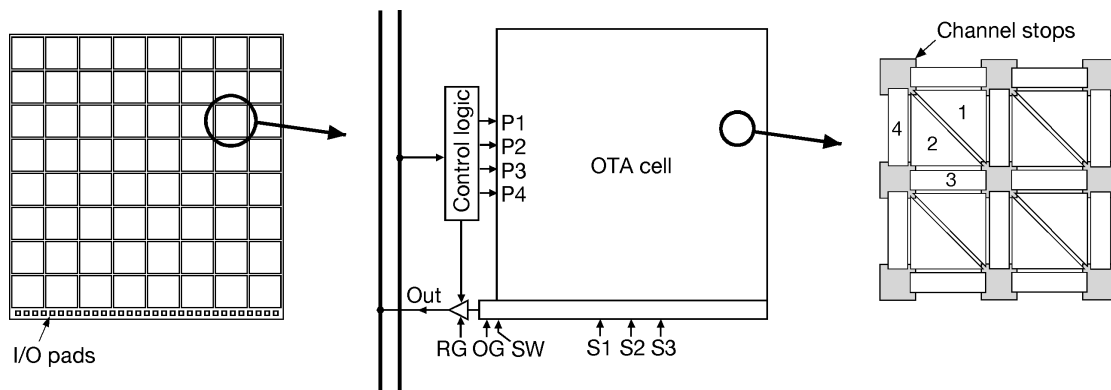


Figure 1. Principal elements of the OTA. Left: the overall chip layout comprising an 8×8 array of OTCCD cells; center: the OTA cell with its control logic; right: one of the OTCCD pixel geometries.

Note that the serial clocks, summing well and reset gate are not under control of the logic. The manner in which the device is to be used allows one set of clocks to feed all cells. These lines are driven by off-chip circuitry.

The operation of the OTA has been previously described^{3, 6} and will be briefly reviewed here with the help of Figure 2. All functioning cells are assigned to either image guide stars for measuring the local image translation or to acquire the science images. Some cells will inevitably be non functional, but the gaps in the science imagery arising from these, as

well as the other non-active regions of the focal plane and the guide star cells, will be filled in by the usual strategy of stacking dithered images.

The first step in imaging a sector of sky is to select those cells, perhaps four or five, that happen to contain sufficiently bright stars to be used as guide stars. These cells will image and read out a small subarray of pixels around the guide star, and from this data the centroids of the stars will be used to construct a map of the image deflection field over the chip FOV. “Sufficiently bright” thus means stars which will yield imagery of sufficient S/N to enable reasonably precise centroiding. This information, in turn, is used to address and update the science cells with the appropriate pixel shifts. The nominal rate at which the cycle of guide-star read and science-cell update occurs is 30 Hz. At the conclusion of the integration period the cells are read out one row at a time through eight video lines that service the eight cells in each column.

One aspect of particular attention in this imager is the speed with which the device could be read out without compromising noise performance. Current astronomical imagers consume large amounts of time, and therefore expense, because of low readout rates. Here we attack the problem by the use of eight parallel output ports and by running the serial read rate at 1 MHz. Work at Lincoln has shown that noise levels below the target level of $5 \text{ e}^- \text{ rms}$ can be achieved at these speeds, though how well we can do in a chip crowded with I/O lines near the video lines and long on-chip video lead lengths remains to be seen. At a 1-MHz read rate the chip can be read out in 2 s, which is a reasonably small fraction of the projected integration time of $\sim 30 \text{ s}$ (Pan-STARRS) and $\sim 200 \text{ s}$ (WIYN ODI).

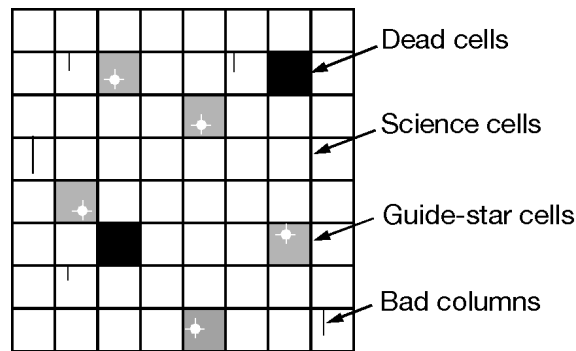


Figure 2. Depiction of the OTA operation.

3. DESIGN AND PROCESS TECHNOLOGY ISSUES

3.1 Process and yield

Both the Lincoln and STA devices are being fabricated with an n-channel CCD process with two levels of metal. One of the main science drivers is a high red response, which in turn dictates thick, back-illuminated devices. The STA OTAs will undergo back-illumination processing at the U. of Arizona Imaging Technology Laboratory. The chemical thinning at UA-ITL requires devices made on p/p^+ epi material, and the highest epi resistivity that could be obtained for the Dalsa processing was $500 \text{ } \Omega\text{-cm}$. Devices made on this material will be thinned to about $25\text{--}30 \text{ } \mu\text{m}$ and should be nearly fully depleted. At Lincoln the substrate material will be $5,000\text{--}10,000 \text{ } \Omega\text{-cm}$ bulk p-type float-zone silicon. Back-illuminated imagers made on such material can be fully depleted at thicknesses as high as $50 \text{ } \mu\text{m}$ under normal operating voltages.

It is our expectation that this device will have a higher yield than a conventional imager of the same area, a critical factor if this device is to be the detector of choice in Gpixel focal planes. This is based on the fact that CCD yields are typically limited by gate shorts that cripple large areas of a device, either by shunting the clock voltages or injecting large amounts of charge into the substrate and creating bright video defects. In this device the effects of such shorts are confined to individual cells, and moreover, such cells can be disconnected from the clock lines by the control logic as described below. On the other hand, the device requires greater process complexity with the addition of control logic and a large number on metal lines on two levels of metallization. We do not expect these features to impact the yield. As described later, the logic requires very few added process steps and does not stress the process technology. The

metal lines were designed with conservative layout rules, and the metal/metal and metal/poly crossovers, which are potential sites for shorts, occupy a rather tiny percentage of the chip area.

3.2 CCD issues

Figure 3 illustrates in more detail the gate layout of the two types of OTCCD cells in the OTA. The pixel layout on the left (type 1) was used in the devices for the OPTIC camera, while the layout illustrated on the right, called the type-2 or “Maltese cross” geometry, has been fabricated only in small devices. In both cases an overflow drain or scupper must wrap around three sides of the pixel array to sink charge transferred beyond the array boundaries. The scupper is also coupled to the input end of the three-phase register to permit flushing of the serial charge in the reverse direction.

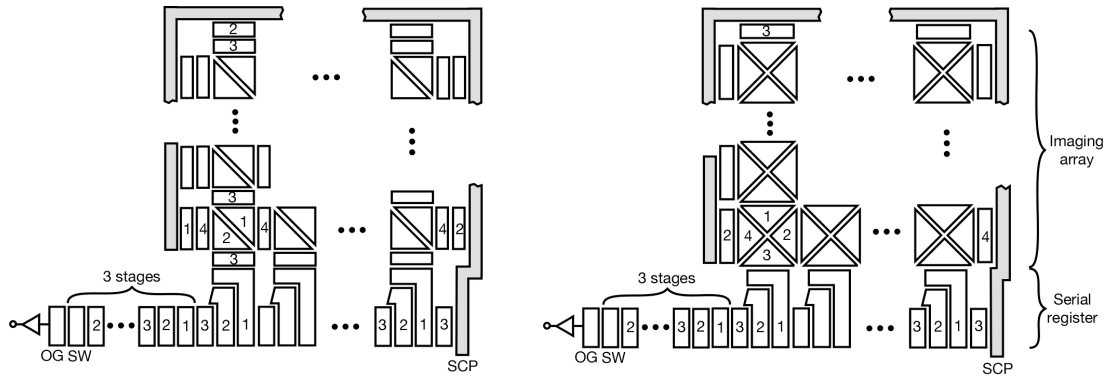


Figure 3. Schematic of the pixel layout for each of the two types of OTCCD cells. The pixel layout on the left is termed the type 1 and that on the right type 2 or Maltese Cross.

Process issues play an important role here in determining the design strategy for the prototype lots, particularly with respect to the pixel size. The OTCCD requires four levels of polysilicon and has a more complex layout than a conventional CCD pixel. Because of this complexity it becomes difficult to scale the pixel size down below about 12 μm without confronting potential yield-reducing process problems. The large ($\sim 20 \text{ cm}^2$) OTCCDs used in the OPTIC camera had 15- μm pixels with the type-1 geometry, and were made at Lincoln with a yield nearly as high as a conventional triple-poly, three-phase device of the same area. For WIYN the desired pixel size is 12 μm (0.11"/pixel), and therefore the STA prototype OTA uses this pixel size together with the proven type-1 geometry. For Pan-STARRS the desired size is somewhat smaller, around 8 to 10 μm (0.22" to 0.28"/pixel). An 8- μm design was deemed too risky at this point and will be deferred, so the approach for the Lincoln prototypes was to design both 12- and 10- μm -pixel devices of the type-1 layout. Although the type-1 pixel has the proven track record, the Maltese Cross has a higher degree of symmetry (potentially more favorable for adaptive imaging) and may well prove to have a higher yield. Therefore two additional OTAs using this design with both 10- and 12- μm pixels were incorporated on the mask set.

3.3 Control logic

The major feature that distinguishes this device from current scientific CCDs is the use of on-chip control logic to independently steer and read out an array of CCD cells. Generally speaking, large scientific CCD imagers do not employ logic devices in order to avoid unnecessary complexity in what is already a difficult device to manufacture. Processes that add CMOS capability to the CCD have been demonstrated but not without additional process complexity. Typically these require thin epitaxial layers on highly doped substrates for the CMOS, which are not compatible with the lightly doped material that is desirable for CCDs to achieve thick depletion layers. However, CMOS processes for high-resistivity material have been described by Holland⁷ and others, as well as a CCD/CMOS process using silicon-on-insulator (SOI),⁸ both of which would allow the CCD to maintain high, broadband quantum efficiency.

In order to add the required circuitry with no reduction in imaging performance and maintain the simplest process, we elected to use NMOS logic. This type of logic was in wide use until the end of the 1970s when its high power consumption lead to its replacement by CMOS. In the OTA the transistor count is sufficiently low that the NMOS

power dissipation is manageable. Of major importance is the fact that NMOS can be added to an n-channel CCD process with very little additional process overhead. Typically only one or two additional ion-implant steps are required, provided the logic devices can perform satisfactorily with the same gate dielectric thicknesses and substrate resistivity as the CCD. The latter requirement is particularly critical, since the CCD must be made on high-resistivity substrates to enable deep depletion layers for enhanced near-IR response. We find that NMOS can be made compatible with such material provided the channel lengths are sufficiently long. In the Dalsa process the gate lengths can be as short as 3.0 μm on 300- $\Omega\text{-cm}$ material, while at Lincoln devices with 4.0- μm gate lengths are known to perform well on material as high as 9000- $\Omega\text{-cm}$.

Figure 4 illustrates the control and readout lines and the logic block associated with each cell. When a logic cell is selected by asserting the corresponding row and column select lines, three data bits, D0–D2, are latched into the cell. These bits set the state of three output control bits, Z0–Z2, which control a set of pass transistors. Bits Z0 and Z1 determine whether each parallel clock phase is set to an active clock line for charge transfer or to one of two standby levels (high, low) during image acquisition. Both bits can be set low to disconnect these gates entirely from the clock lines, a feature that will prove useful for dealing with cells that have serious gate shorts. Such shorts might otherwise place a severe load on the clock lines or inject large amounts of charge into the substate.

The Z2 bits determine which output video signals are multiplexed onto each of eight column video out lines. Because all the cells in a column share a single video-out bus we are constrained to reading only one cell per column at a time. The design goal for the serial read rate is 1.0 MHz, which, combined with the relatively long video-output lines, requires a two-stage source follower for the CCD output amplifier.

Most of the logic is designed to run at a supply voltage of 5.0 V. The pass transistors driven by the Z0–Z2 lines need to be driven by somewhat higher voltages to allow parallel clock swings of as much as 10–12 V and to switch the video output from the source followers. Consequently, the logic gates that supply these levels operate from a separate 12.0-V supply. We estimate an average power dissipation for the entire chip of about 300 mW for the logic and another 300 mW from the source followers.

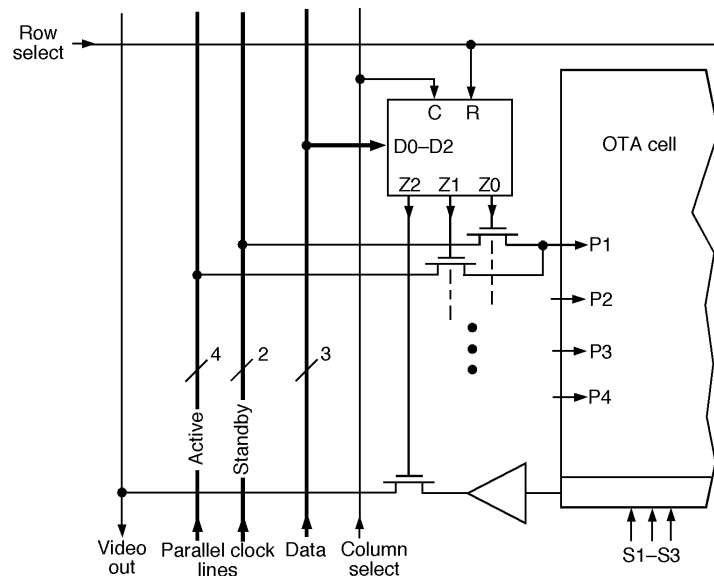


Figure 4. Arrangement of control lines and logic for each OTA cell.

4. PACKAGING TECHNOLOGY AND GIGAPIXEL FOCAL PLANE

The OTA is intended to be used in 1-Gpixel focal planes consisting of about 60 chips each. One of the main goals for this, or any astronomical, focal plane is maximizing active area or fill factor. A number of steps have been taken to

avoid unnecessary dead space in the final focal plane, first, by ensuring minimal seam loss between the cells on each chip and second, by using a carefully designed four-side-abutable package.

As mentioned earlier, the OTCCD cells in the first prototype design are abutted as much as the process technology allows while maintaining reasonably conservative design rules. Space has to be allocated for the logic block and the output amplifier to the left of each cell, and the serial register on the bottom. In addition, metal I/O lines must criss-cross the chip in the “streets” between the cells, and space must be set aside for I/O pads. In the first prototype device the chip fill factor is about 0.90, with nearly 40% of the dead space due to the metal lines running vertically between cells. One design variant being tried on some wafers is to take the digital control lines (but not the low-noise analog lines) out of the streets and place them on top of the pixel array. For a back-illuminated device there is obviously no issue here with obscuration of the pixels, though the metal will no doubt introduce some change in sensitivity to deeply penetrating near-IR photons. This approach will boost the fill factor to almost 0.92, but with the risk of a possible yield reduction due to metal/pixel-array shorts.

The OTA package with an OTA chip mounted on it is shown in Figure 5. The package design has a proven heritage with a similar design for the Hawaii-2RG IR sensors. A Mo plate serves as the base of the package. The CCD is epoxied to the front surface of this plate, while the back has three threaded holes for alignment feet and clips for attaching a wirebond ceramic PGA. The feet enable kinematic mounting of the package to the focal-plane assembly as well as the thermal path for cooling the device.

The ceramic PGA provides bond pads for the chip I/O and pins for attaching a flexprint. The bond pads occupy a ledge that protrudes approximately 1.7 mm beyond the edge of the die/moly base. Because this ledge and the corresponding pad real estate on the chip contribute a significant amount to the total focal-plane dead space, we elected to keep all I/O on one edge. The exposed ledge contributes 1.7/50 or 3.4% to the loss, so that the net fill factor for the first versions of the focal plane will be about 0.87, assuming no gap between adjacent packages.

This ceramic uses multi-layer thick-film construction with four internal metal layers plus the two exposed layers for routing signals from the pads to the PGA pins. In addition, several common signals from the CCD are joined to reduce the 99 CCD I/O leads to 71 pins on the PGA. Bypass capacitors and JFET buffers are also located on the ceramic.

Figure 6 illustrates the 1-Gpixel focal plane (GPC) with 64 OTAs for both Pan-STARRS and the WIYN ODI.

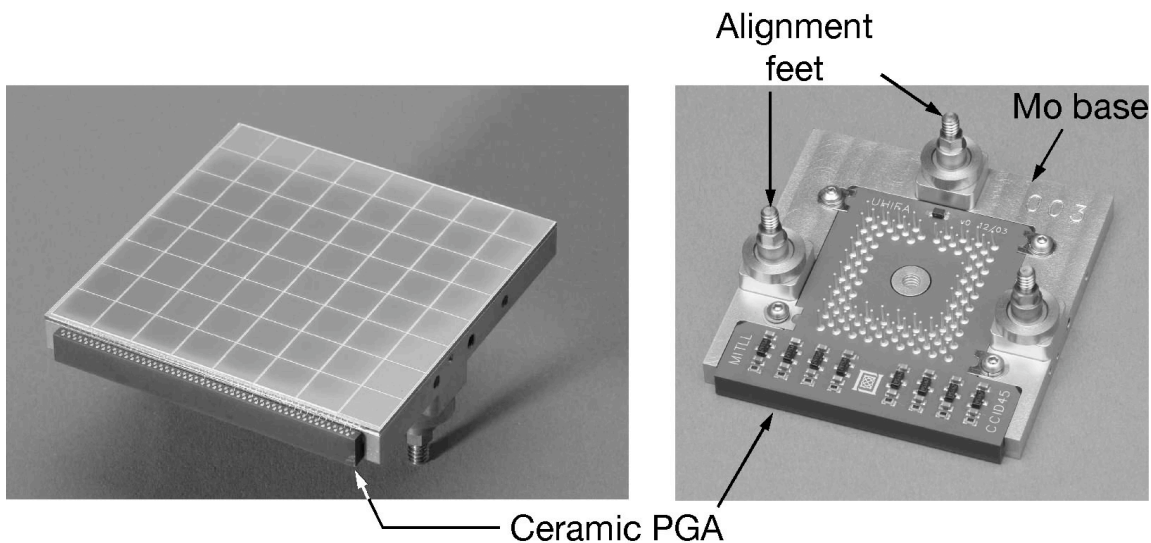


Figure 5. Photograph of a packaged OTA (left) and bottom view of the package (right).

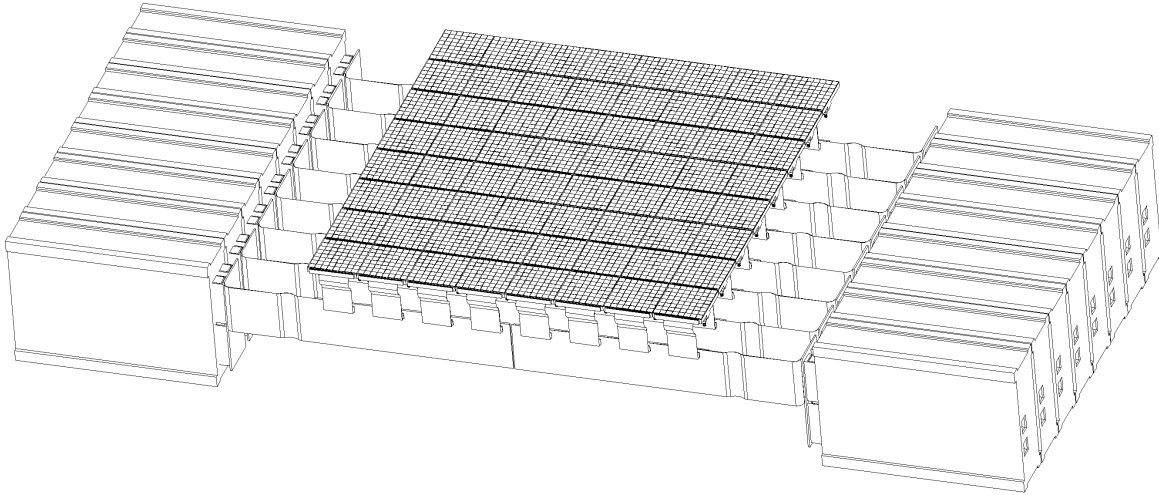


Figure 6. Conceptual drawing of the 64-chip focal plane and electronics for Pan-STARRS and the WIYN ODI. The flexprints which attach to the PGA on the bottom of the package can be seen. These in turn are attached to a set of eight flexprints running horizontally through the cryostat walls to the drive electronics modules.

5. CURRENT STATUS

At this writing the first wafer lots are complete both at Lincoln and Dalsa and wafer probing is under way. Figure 7 shows a closeup of one portion of an OTA at the intersection of four cells. A large number of vertically running metal lines can be seen, most of which carry the logic power, data, and parallel clock voltages and the remainder the source follower power and video output lines. The horizontal metal lines between the cells are the serial clocks and the row address lines.

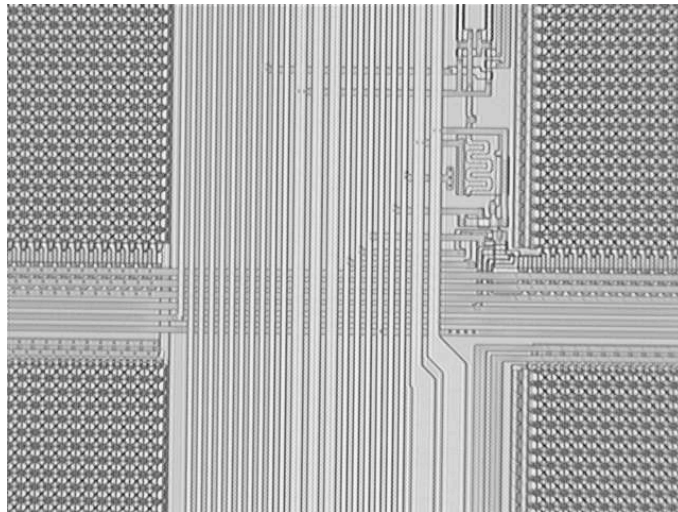


Figure 7. Photograph of a portion of one of the OTAs on the Lincoln wafer lot. The area shown here is the intersection of four of the cells, and shows the horizontal and vertical metal lines running in the streets between cells. The output circuit and a portion of the logic can be seen to the left of the upper right cell.

6. SUMMARY

A novel CCD imager architecture, the orthogonal-transfer array or OTA, has been designed in a collaborative effort between the Pan-STARRS program at the U. of Hawaii and the WIYN observatory. Fabrication of the first prototype designs, carried out at MIT Lincoln Laboratory and Semiconductor Technology Associates, are complete and in test. This device will enable wide-field, tip-tilt-corrected imagery, and will be incorporated into 1-Gpixel focal planes.

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